REMARKS

Claims 1-24 are pending. Claims 1, 5, 7, 8, 12, 13, 17, 19, 20 and 24 are being amended, and claims 2-4, 6, 9-11, 14-16, 18 and 21-23 remain unchanged. Claims 5 and 17 are rejected under 35 U.S.C. § 112 as allegedly being indefinite. Claims 1-24 are rejected under 35 U.S.C. § 102 as allegedly being anticipated by U.S. Patent No. 5,742,782 issued to Ito et al. (herein referred to as "Ito").

Formal Matters

Claims 7, 12, 19 and 24 have been amended for improved readability by reciting "first" and "second" registers, instead of "third" and "fourth" registers." This amendment does not alter the scope of claims 7, 12, 19 and 24.

Rejections Under 35 U.S.C. § 112

Claims 5 and 17 have been amended in view of the Examiner's comments. As amended, claims 5 and 17 are believed to overcome the rejection under § 112.[1]

Rejections Under 35 U.S.C. § 102

Claim 1

Applicants respectfully submit that Ito fails to anticipate claim 1. Claim 1 relates to a SINGLE instruction specifying an operation that is to be performed on each one of a plurality of data elements in partitioned fields of at least one register. By contrast, Ito discloses a traditional technique for MULTIPLE instructions to operate on data stored in separate registers. It is believed that even without the current amendment, claim 1 clearly distinguishes from the multiple-instructions technique of Ito. However, in the interest of expediting prosecution of the

[1] Applicant respectfully submit that one of ordinary skill in the art of would understand that, even as originally claimed, the limitation that only one thread can handle an exception at any given time refers to the requirement that only one thread can have an exception that is handled (such as by an exception handler routine) at any given time. However, claims 5 and 17 have been amended to expedite prosecution by clarifying the recited limitations.

present application, claim 1 has been amended to further highlight the significant difference between the present invention and Ito. As amended, claim 1 recites:

> "each instruction stream including a single instruction that specifies an operation, the operation to be performed on each one of a plurality of data elements in partitioned fields of at least one of the registers to produce a catenated result" (emphasis added)

Ito fails to disclose such a single instruction that specifies an operation that is to be performed on each one of a plurality of data elements in partitioned fields of at least one register. Ito describes a traditional technique requiring multiple instructions that specify different operations to be performed on data in separate registers. Fig. 8 of Ito, which is cited by the Examiner and is reproduced below, clearly illustrates Ito's multiple instructions:

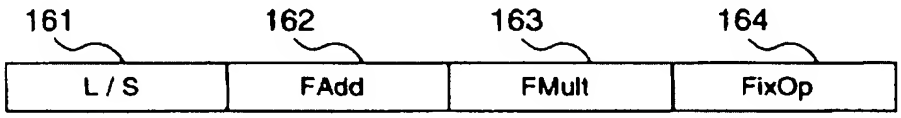

Fig. 8 of Ito

As seen in this figure, Ito discloses multiple instructions, namely 4 instructions: (1) an "L/S" instruction, (2) an "FAdd" instruction, (3) an "FMult" instruction and (4) a "FixOp" instruction. These 4 instructions specify 4 different operations that are performed on data stored in separate registers. The "L/S" instruction specifies a load/store operation performed on data in a first set of registers. The "FAdd" instruction specifies a floating-point add operation performed on data in a second set of registers. The "FMult" instruction specifies a floating-point multiply operation performed on data in a third set of registers. The "FixOp" instruction specifies an integer operation performed on data in a fourth set of registers. See Ito, col. 4, lines 9-22. The four sets of registers are specified by four sets of "source 1 register number holding latches" (175) and "source 2 register number holding latches" (176) shown in Fig. 6 of Ito. See Ito, col. 13, lines 33-49. Thus, Ito's 4 instructions specify 4 completely different operations to be

performed on data in different registers. In fact, Ito employs 4 different execution devices that independently perform these 4 different operations so as to not interfere with one another. See Ito, col. 6, lines 27-29 ("An the respective instruction execution parts 25 are operated independently without interference with each other").

Thus, Ito merely discloses a traditional technique of using 4 instructions to specify 4 different operations that are performed on different data in separate registers. None of the 4 operations is performed on each one of a plurality of data elements stored in partitioned fields of at least one register. Instead, each of the 4 operations is performed on its own set of data stored in its own set of registers. This clearly fails to teach the use of a single instruction to specify an operation, wherein the operation is performed on each one of a plurality of data elements stored in partitioned fields of at least one register. For at least this reason, Ito fails to anticipate claim 1.

Furthermore, Ito also fails to disclose an operation that is performed on each one of a plurality of data elements to produce a catenated result, as recited in claim 1. As mentioned previously, Ito discloses 4 instructions that specify 4 completely different operations to be performed on data in separate registers. These 4 different operations independently generate 4 individual results that are never catenated together. Instead, the 4 individual results are written to 4 separate destination registers. The 4 destination registers are specified by four sets of "destination register number holding latches" (177) shown in Fig. 6 of Ito. See Ito, col. 13, lines 50-55. By writing the 4 individual results to separate registers, Ito not only fails to disclose, but in fact teaches away from, the production of a catenated result. For this additional reason as well, Ito fails to anticipate claim 1.

Thus, Ito discloses multiple instructions which specify different operations performed on different data to produce individual results that are never catenated together. Such a technique

fails to disclose various novel features of claim 1 as, as discussed above. Accordingly, Ito cannot anticipate claim 1.

Claims 2-5

Claims 2-5 depend from claim 1 and therefore incorporates all of its limitations. As such, for at least the reasons discussed above with respect to claim 1, Ito also fails to anticipate claims 2-5.

Claim 6

Claim 6 depends from claim 1 and therefore incorporates all of its limitations. As such, for at least the reasons discussed above with respect to claim 1, Ito also fails to anticipate claim 6. Furthermore, claim 6 recites:

> "The processor of claim 1 further comprising a virtual memory addressing unit and a cache operable to store data communicated between the external interface and the data path" (emphasis added)

Ito fails to disclose a virtual memory addressing unit as recited in claim 6. The Examiner does not point to any portion of Ito as supposedly disclosing a virtual memory addressing unit. Instead, the Examiner only makes the conclusory statement that "[it is] certainly existing in Ito et al. '782's system for handling input/output operation of peripherals." See Office Action dated 4/24/06, p. 6, first paragraph. However, the handling of input/output operations of peripherals is merely a general feature often found in computer systems, and it says nothing about whether the system includes a virtual memory addressing unit. Indeed, there is absolutely no disclosure or even remote suggestion of a virtual memory address unit in Ito. For at least this additional reason, Ito cannot anticipate claim 6.

Claim 7

Claim 7 depends from claim 1 and therefore incorporates all of its limitations. As such, for at least the reasons discussed above with respect to claim 1, Ito also fails to anticipate claim 7. Furthermore, claim 7 as amended recites:

> "multiply the plurality of floating point operands in the first register by the plurality of operands in the second register to produce a plurality of products and provide the plurality of products to partitioned fields of a result register as a second catenated result" (emphasis added)

Ito fails to disclose these features of claim 7. As discussed previously, Ito's traditional technique involves operations performed on data in separate registers, not partitioned fields of a register. Also, Ito's results are written to separate registers, not partitioned fields of a result register. For example, for a floating point multiply operation, Ito's system multiplies two floating-point numbers separately stored in two source registers. The product that is generated is written to a separate destination register. See Ito, Fig. 9 and col. 4, lines 45- 55 ("As shown in FIG. 9, each of the FAdd, FMult and FixOp instructions is made up of fields of an opecode, a destination (destination register number), an empty field, a source 1 (source 1 register number) and a source 2 (source 2 register number[)]. The execution of this instruction is to perform an operation designated by the opecode field over the values of registers designated by the sources 1 and 2 fields and to store the operation result in the destination register").

That is, in the Ito system, each source operand register contains only one operand for the multiply operation, and each destination register contains only one product produced from the multiply operation. Thus, Ito's system clearly fails to disclose a "plurality of operands in the first register." Similarly, Ito fails to disclose a "plurality of operands in the second register." Finally, Ito fails to disclose "provid[ing] the plurality of products to partitioned fields of a result register." For at least these additional reasons as well, Ito fails to anticipate claim 7.

Claim 8

Claim 8 is rejected based on the same rationale as claim 1. For at least similar reasons as stated above with respect to claim 1, Ito also fails to anticipate claim 8.

Claims 9-11

Claims 9-11 depend from claim 8 and therefore incorporate all of its limitations. As such, for at least the reasons discussed above with respect to claim 8, Ito also fails to anticipate claims 9-11.

Claim 12

Claim 12 depends from claim 8 and therefore incorporates all of its limitations. As such, for at least the reasons discussed above with respect to claim 8, Ito also fails to anticipate claim 12. Furthermore, claim 12 is also rejected based on the same rationale as claim 7. Thus, Ito fails to anticipate claim 12 for at least similar reasons as stated above with respect to claim 7, as well.

Claim 13

Claim 13 is rejected based on the same rationale as claim 1. For at least similar reasons as stated above with respect to claim 1, Ito also fails to anticipate claim 13.

Claims 14-17

Claims 14-17 depend from claim 13 and therefore incorporate all of its limitations. As such, for at least the reasons discussed above with respect to claim 13, Ito also fails to anticipate claims 14-17.

Claim 18

Claim 18 depends from claim 13 and therefore incorporates all of its limitations. As such, for at least the reasons discussed above with respect to claim 13, Ito also fails to anticipate claim 18. Furthermore, claim 18 is also rejected based on the same rationale as claim 6. Thus,

Ito fails to anticipate claim 18 for at least similar reasons as stated above with respect to claim 6, as well.

Claim 19

Claim 19 depends from claim 13 and therefore incorporates all of its limitations. As such, for at least the reasons discussed above with respect to claim 13, Ito also fails to anticipate claim 19. Furthermore, claim 19 is also rejected based on the same rationale as claim 7. Thus, Ito fails to anticipate claim 19 for at least similar reasons as stated above with respect to claim 7, as well.

Claim 20

Claim 20 is rejected based on the same rationale as claim 1. For at least similar reasons as stated above with respect to claim 1, Ito also fails to anticipate claim 20.

Claims 21-23

Claims 21-23 depend from claim 20 and therefore incorporate all of its limitations. As such, for at least the reasons discussed above with respect to claim 20, Ito also fails to anticipate claims 21-23.

Claim 24

Claim 24 depends from claim 20 and therefore incorporates all of its limitations. As such, for at least the reasons discussed above with respect to claim 20, Ito also fails to anticipate claim 24. Furthermore, claim 24 is also rejected based on the same rationale as claim 7. Thus, Ito fails to anticipate claim 24 for at least similar reasons as stated above with respect to claim 7, as well.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael A. Messina
Registration No. 33,424

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MAM:DAB
Facsimile: 202.756.8087
Date: October 24, 2006

Please recognize our Customer No. 20277 as our correspondence address.